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SIGMA RESEARCH INC RICHLAND WA MAR 81 DAAK51-80-C-0023

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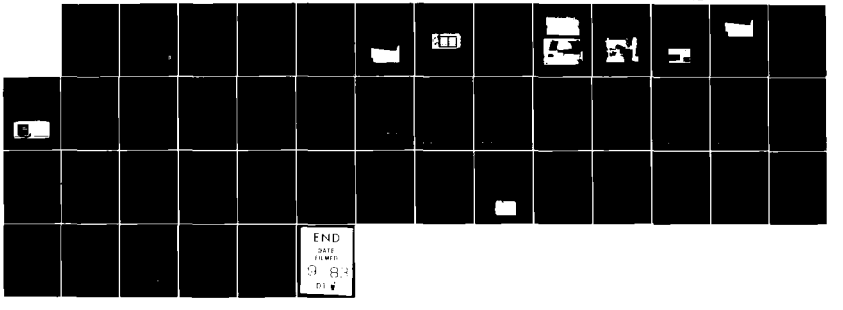

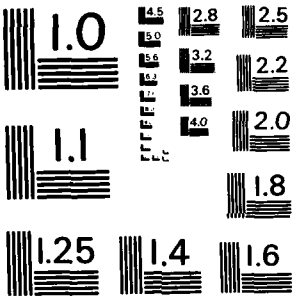

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FINAL REPORT

Contract No. DAAK51-80-C-0023

(2)

PLASMA-SPRAY COATING THICKNESS MONITORING SYSTEM

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LEWIS RESEARCH CENTER
21000 Brookpark Road
Cleveland, OH 44135

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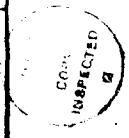

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Section 1

PRINCIPLES OF OPERATION

The Plasma-Spray Coating Thickness Monitoring System ~~(Figure 1) built by Sigma Research, Inc.,~~ incorporates a unique optical transform technique that enables an image of a coupon (part) surface to be projected on a one-dimensional linear diode array (LDA). Parts to be coated with plasma spray are mounted on a carousel, and a probe containing the optics and LDA is attached to one side. The system measures the height of the coupon surface, thus providing a way to determine the thickness of the ceramic coating. The optical pattern impressed on the diode array is converted to an accurate representation of coating thickness by a small microprocessor-based control and readout console mounted adjacent to the equipment operator.

Although the environment surrounding a plasma spray gun is acoustically and electrically noisy, Sigma's system performs well with minimal maintenance. The electronics are removed from the carousel area, and only the rugged optical components are in close proximity.

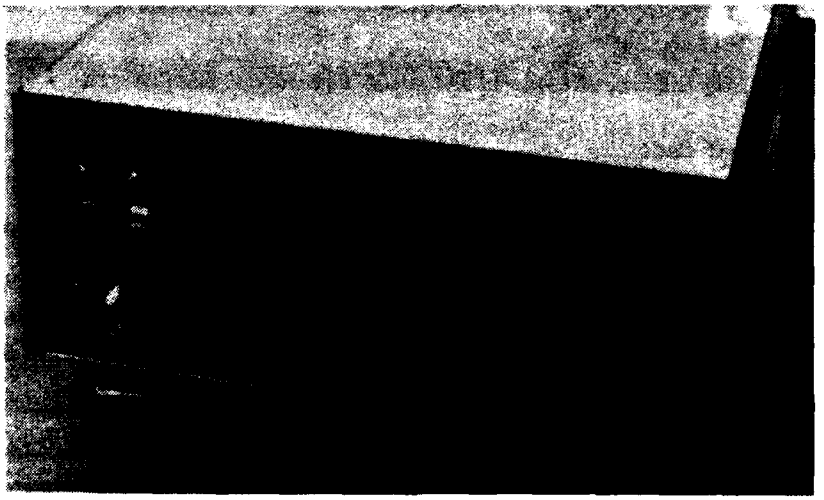


Figure 1. Plasma Spray Thickness Monitoring System

ELECTRONICS

The electronics consist of three circuit boards located in a card cage inside the cabinet (see Figure 2). A Reticon RC100B board (Figure 2, Item 1 and Appendix A) in the card cage is used in combination with an RC105 board in the probe to control the RL512G LDA. The processor board (Figure 2, Item 2 and Appendix B) is a Pro-Log PLS-898 with a Z-80 microprocessor, 4 k of read-only memory (ROM), and 1 k of random access memory (RAM). A custom interface board contains the interface and input/output (I/O) logic (Figure 2, Item 3). (See Drawing 3291-700, Sheets 1 and 2, Appendix C, for further information.)

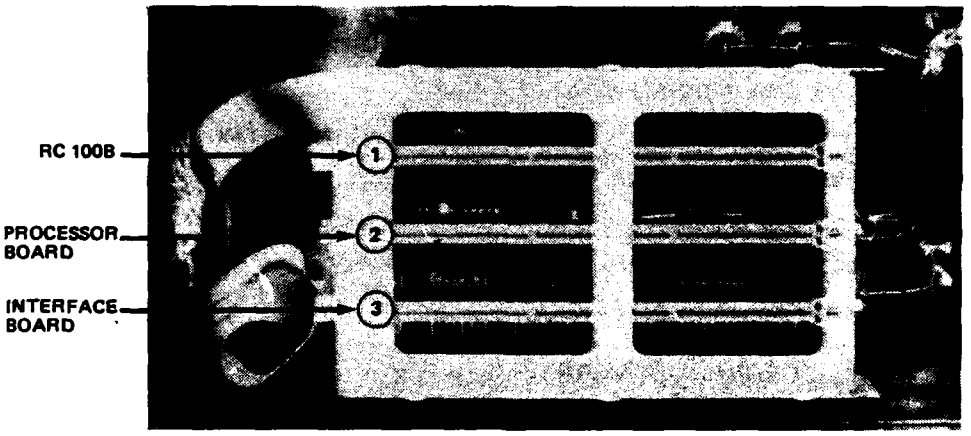


Figure 2. Card Cage

As a slot in the carousel position encoding disc passes between the emitter and detector, the coupon position detector generates a pulse, which is squared by a Schmidt trigger that fires a one-shot delay that sets the interrupt generator flip-flop. This generates an interrupt that, when acknowledged by the microprocessor, is reset; then, the processor sends a start signal to the start-signal generator, which is synchronized with the clock for the RC100B board.

This signal provides the external start pulse for the RC100B as well as the external scope sync. A start acknowledge is also fed back to an input port for verification by the processor, which initiates sequential sampling of each of the 512 diodes in the array. The "Clock Out" pulse generates a 60 μs convert pulse for the analog-to-digital converter (ADC), an AD 570. The video output is scaled by an LM318 OP Amp and is sampled by the ADC and made available at the video-out connector.

The "Data Ready" pulse from the ADC sets the Data Ready flip-flop, which is reset when the processor acknowledges the data. The processor also interrogates the switch positions to set the desired operating mode and outputs data to the display on the front panel.

Data to and from the probe are transmitted by current drivers and coaxial cables through an EMI/RFI-shielded (electromagnetic interference/radio frequency interference) conduit. Thermoelectric coolers are installed in the probe to keep the LDA cool because dark current doubles for each 6°C increase in temperature. A dry nitrogen purge also helps cool the probe and keeps the inside of the probe and the window clean. This purge is also neccessary to prevent condensation on the cooled LDA.

The RC105 card in the probe (see Figure 3) is enclosed in an Amuneal box within the aluminum housing for EMI/RFI shielding. Special care was taken to shield the electronics by putting the card cage in a double-walled copper-Amuneal box (Figure 4); and the fan filter, exhaust vent, and display window are also EMI/RFI-shielded. All electrical interconnects are filtered feed-throughs.

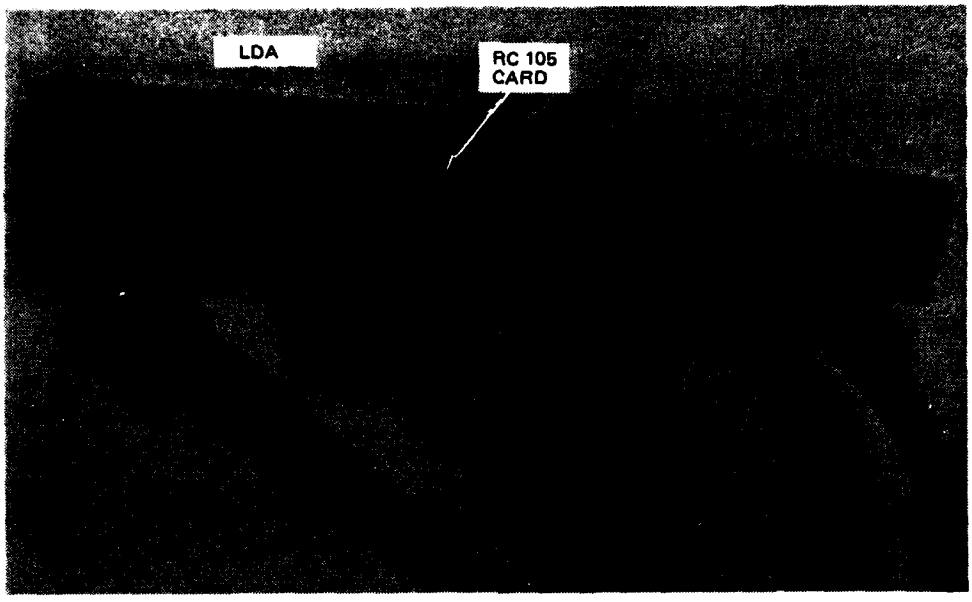


Figure 3. Probe

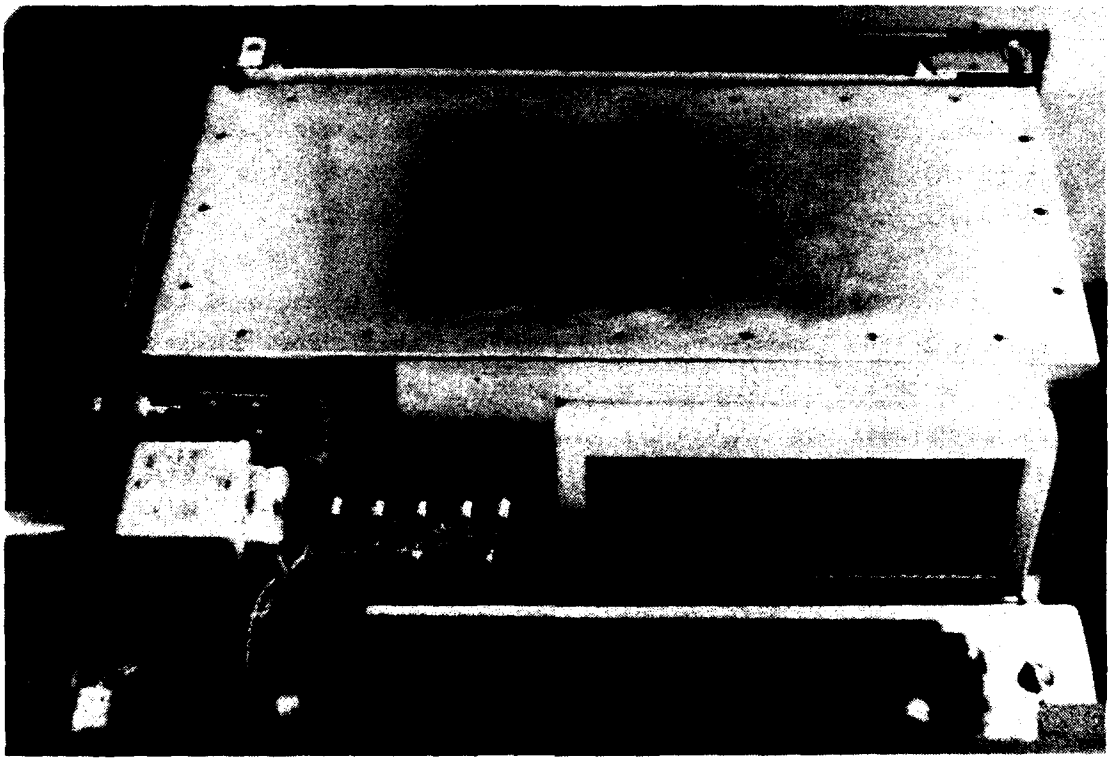


Figure 4. EMI/RFI-Shielded Box

The probe is permanently attached by a 15-ft cable bundle within the shielded conduit that also contains the fiber optic transmission from the laser. The optical fiber shines a laser spot on the surface being measured. Figure 5 shows the calibration setup. A lens within the probe images the spot through an RFI-filtered window--and a bandpass filter to filter out room light--onto the LDA. Position is determined by the distance of the spot from the probe on a 1-to-1 basis; i.e., a 0.002-inch movement moves the image 0.002 inch on the LDA (two diode positions). Slight nonlinearity is eliminated by a ROM-based look-up table within the microprocessor; thus, the instrument is inherently accurate and requires no calibration adjustment (see Appendix D).

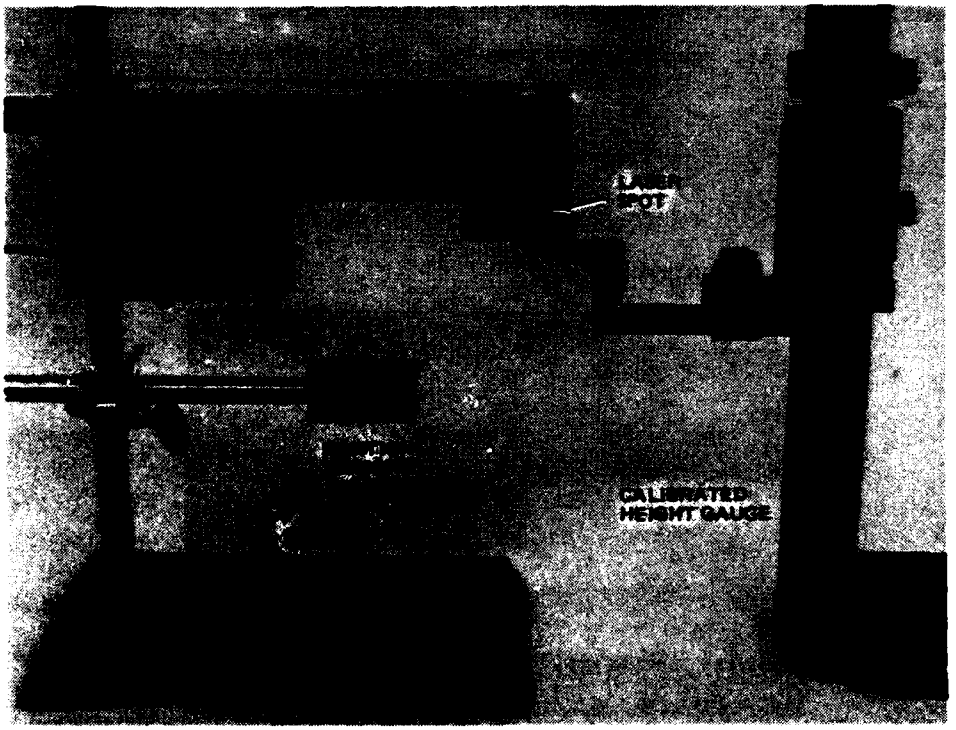


Figure 5. Calibration Setup

ADJUSTMENTS

Adjustments are provided for the video gain and offset using 200-k and 5-k potentiometers, respectively, on the video amplifier (IC5). The only other adjustments are for the Reticon LDA control board, which are described in the Reticon Manual (Appendix B).

One mechanical adjustment is required to adjust the laser spot intensity. This can be done by loosening the laser (Figure 6) and tilting it up to reach the fiber optic mount (Item 1). Place a sample coupon (or white paper) under the probe with the test switch on. Adjust the position to its midpoint location or 256 on the display. Monitor the video output and adjust the positioning of the fiber until the top of the video signal starts to be clipped off; then, back off so there is no clipping. Three mounting screws (Item 2) can be loosened with an Allen wrench. Position the fiber optic mount to its optimum position within the oversize holes and retighten the screws.

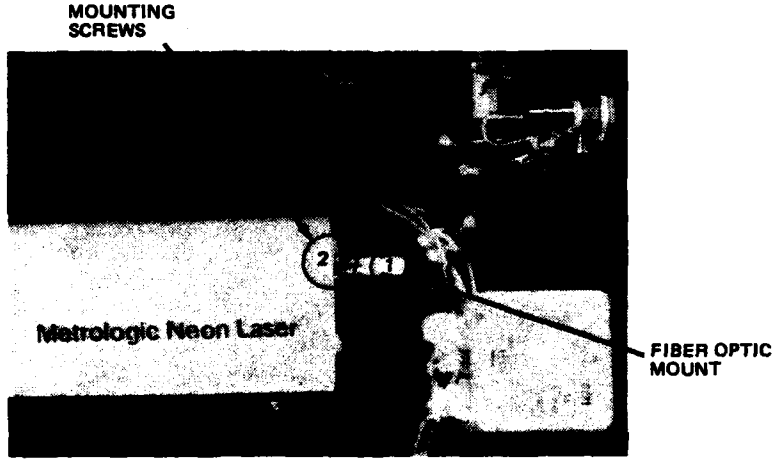


Figure 6. Laser

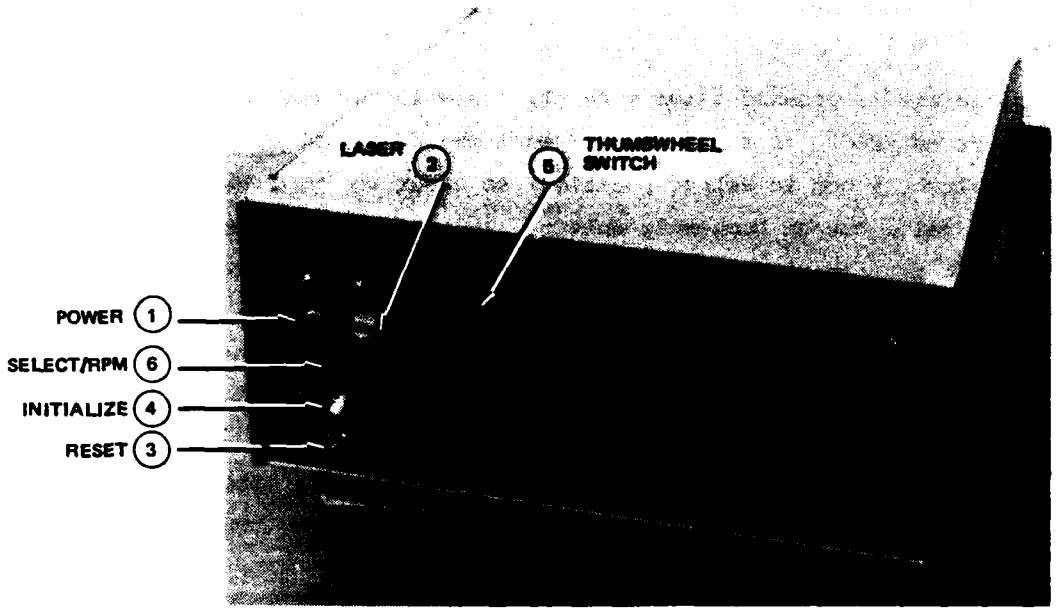


Figure 7. Front Panel

FUNCTION OF CONTROLS (See Figure 7)

Power (Item 1)

This control turns the power on.

Laser (Item 2)

This key switch control energizes the laser.

Reset (Item 3)

This button can be pushed at any time and causes the same functions to be performed as a power-up sequence. After a reset, "888" shows on the display for a few seconds as a test of the display circuitry. The rotation speed of the carousel is measured and displayed in revolutions per minute (rpm). An error "␣00" will be displayed if the carousel is not turning. Errors will also result if the carousel speed is altered during a run. Selecting RPM on the Select/RPM switch will remove these errors without resetting the zero thickness if the speed needs to be altered for some reason.

Initialize (Item 4)

If Initialize is pressed after a reset, the value of the thumbwheel switch will be entered. If a number between 1 and 12 is not selected or the Select/RPM switch is not in Select position, an error of "␣00" will be displayed. If a valid coupon number is entered, this number will be displayed while eight (8) readings are taken and averaged. When this is finished, zero will be displayed and spraying can begin. The coupon being monitored will not change until the next Reset, regardless of the setting of the thumbwheel switch.

If the Initialize button is held in continuously, scans will be taken continuously without waiting for the correct coupon position. This allows the device be used as an optical micrometer.

Selector Thumbwheel (Item 5)

This switch is read at the time Initialize is pushed and selects a coupon to monitor. The Select/RPM switch must be in Select position. After initialization, this switch is used to select a display function.

Position Switches

1-12. The thickness in mils, relative to the initial measurement, is displayed for the coupon selected. This thickness is the absolute value of difference between the current measurement and the initial measurement. This value is the average of the most recent eight readings to minimize flicker.

13. The pulse width is displayed. This is the number of diode positions between the half-maximum points of the intensity distribution on the LDA.

14. This is the magnitude of the signal into the A/D converter for the diode at the calculated spot position and can be interpreted as pulse height.

15. This is the calculated position of the spot of light on the diode array.

0. One revolution is timed, and the rotation rate in rpm is displayed.

Select/RPM (Item 6)

On RPM, the Selector switch is overridden and a zero is forced for the selector.

Test (See Figure 8, Item 1)

This toggle switch is located on the back of the unit and performs the same function as holding the Initialize pushbutton.

Outputs (Figure 8)

Two BNC connectors are provided on the back of the unit. A positive start pulse is provided at the Sync output (Item 2), and the 35-ms video signal from the LDA is available at the Video output (Item 3).

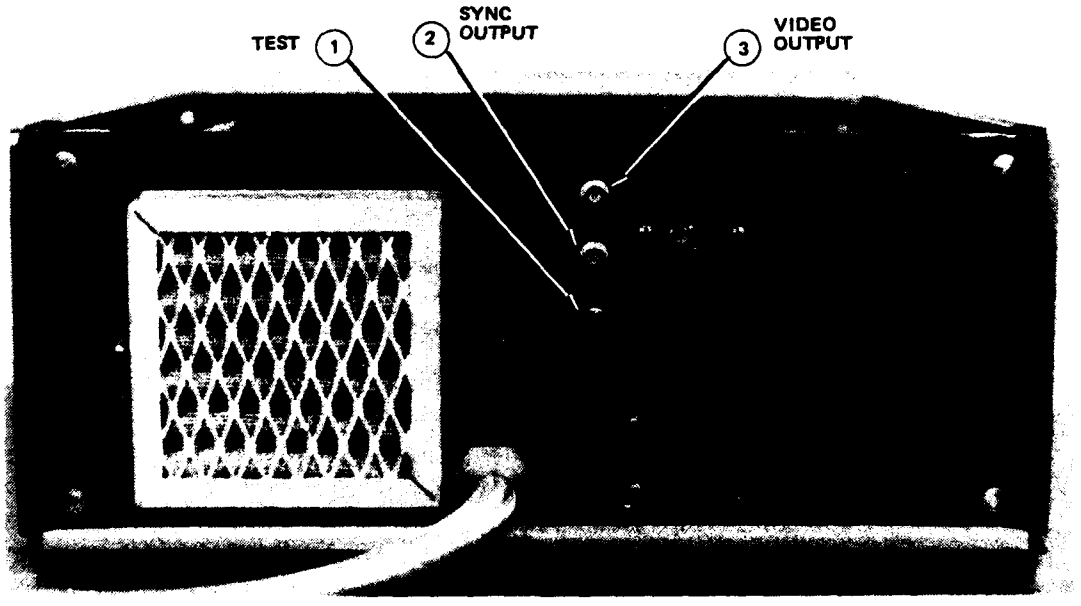


Figure 8. Rear Panel

Section 2

SETUP PROCEDURE

The probe and position sensor must be set up properly prior to turning the instrument on.

1. Position sensor must be positioned so that the disc rides as far as possible within the slot without touching the sensor.

NOTE

INSTALL THE DISC SO THAT IT IS CONCENTRIC WITH THE CAROUSEL AND IS NOT WARPED.

2. Position probe above carousel.

NOTE

RELATIVE POSITION OF SENSOR AND PROBE MUST BE SO THAT THE SENSOR LEADS THE PROBE BY APPROXIMATELY ONE-HALF THE DISTANCE BETWEEN TWO SPECIMENS IF THE HOLES IN THE SENSOR DISC ARE DIRECTLY BELOW THE SPECIMEN. AN ALTERNATIVE WOULD BE TO ROTATE THE SENSOR DISC SO THAT THE HOLES FALL BETWEEN THE SPECIMENS. IN THIS CASE THE POSITION SENSOR SHOULD BE DIRECTLY BELOW THE PROBE.

3. Adjust height:

   a. Turn on "test" switch on back panel.

   b. Rotate carousel so lowest specimen is under the probe.

   c. Turn on power and laser.

   d. Set thumbwheel switch to 15.

   e. Press reset.

   f. Adjust height of probe so that display reads between 400 and 450.

Section 3

NORMAL OPERATING PROCEDURE

1. Turn on carousel, measuring device, and laser.

NOTE

BE SURE THAT THE TEST SWITCH ON THE BACK PANEL IS NOT IN THE TEST POSITION.

2. When carousel has constant speed, push Reset.

3. Switch Select/RPM to Select position.

4. After "888" and RPM are displayed, select coupon number to be monitored on thumbwheel switch and press Initialize.

NOTE

THE COUPON SELECTED WILL BE DISPLAYED UNTIL 8 READINGS ARE TAKEN AND AVERAGED TO CALCULATE THE ZERO THICKNESS REFERENCE. WHEN READY, A ZERO WILL BE DISPLAYED.

MICROMETER OPERATION

1. Turn on measuring device and laser; switch back panel switch to Test position.

2. Push Reset to set zero position measurement.

3. Selector positions 1-12 will display changes in thickness.

4. Other positions have the same definitions as before.

ERROR CODES

If an error is detected, the display will show "␣0n" where n is a number between 0 and 5. The following table shows the meaning of each code.

Table 1

ERROR CODES

0	Invalid coupon number. Reset and select coupon number. Make sure SELECT/RPM switch is in Select position.
1	Coupon surface is not in measuring range or spot intensity is too small.
2	Start Acknowledge was not received after start was sent. Electronic problem with scanning circuitry is a likely cause.
3	Unused.
4	Number 1 marker was not detected after coupon 12. Carousel speed may not be constant. Try RESET.
5	Number 1 marker detected but not after coupon 12. Carousel speed may not be constant. Try RESET.

DATA FORMAT

The output of the A/D comes through port 0. These data will begin arriving about 70 μsec after a start pulse is sent by the computer. The start pulse is sent by pulsing bit 0 of output port 2; then, the computer clears the Data Ready flip-flop and waits for a Data Ready pulse. When data are read, clear Data Ready and wait some more. Do this until 512 pulses come.

If there is an interval greater than 200 μs between the start pulse and a start acknowledge, error "␣02" will result.

PROXIMITY DETECTOR REQUIREMENTS

A ring with holes drilled in it is provided to identify the location of the coupons and identify number one. Twelve slots are spaced evenly around the edge, and number one is identified by an extra slot less than one-half the normal slot spacing after number one. The scan begins midpoint between the markers and lasts for 70 ms. At 20 rpm, this is 8.4° of rotation or 1.03 inches of arc at a 7-inch radius.

The sensor itself is an LED-photo transistor pair. The output is a negative-going pulse that must be less than 25 ms long. The normal state needs to be greater than 3 volts and the "sense" state should be less than 2 volts.

APPENDIX A
RETICON RC-100B SERIES CIRCUIT BOARDS ALIGNMENT PROCEDURE

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED

RC-100B SERIES CIRCUIT BOARDS ALIGNMENT PROCEDURE

GENERAL DESCRIPTION
INTERNAL/EXTERNAL CLOCK OPERATION
INTERNAL/EXTERNAL START OPERATION

SECTION I — RC100B MOTHERBOARD WITH RC-101, 102, OR 103 AND FOUR PHASE "C" ARRAY

SECTION II — RC-100B MOTHERBOARD WITH RC-101, 102 OR 103 WITH "EC" ARRAY

SECTION III — RC-100B MOTHERBOARD WITH RC-104, 105 OR 106 AND "G" SERIES ARRAY

SECTION IV — RC-100B MOTHERBOARD WITH RC-107 OR 108 AND "H" SERIES ARRAY

SECTION V — RC-100B MOTHERBOARD WITH RC110-2 WITH RA32x32A ARRAY OR RC110-1 WITH RA50x50 ARRAY

SCHEMATIC — SCHEMATIC DIAGRAM, MOTHERBOARD, RC-100B, 011-0238

ASSEMBLY — ASSEMBLY DIAGRAM, MOTHERBOARD, RC-100B, 010-0238

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	RETICON RETICON CORPORATION 910 Benecia Ave. Sunnyvale California 94086	
	APPROVALS / DRAWN	DATE 2-24-78	RC-100B SERIES CIRCUIT BOARDS ALIGNMENT PROCEDURE
MATERIAL	CHECKED		
FINISH			SIZE A / CODE IDENT NO. / DRAWING NO. 045-0050
DO NOT SCALE DRAWING			SCALE / SHEET 1 OF 9

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4166

GENERAL DESCRIPTION

The Reticon RC-100B series circuit provides all clock, start, video amplifier, and blanking requirements for Reticon C, EC, G, H, and some RA series photodiode arrays.

Each circuit consists of two printed circuit boards -- an RC-100B "Motherboard", approximately 4.5 x 6 inches in dimension, which contains the clock and start generators, blanking circuit, sample-and-hold circuit, and buffer amplifiers, and the array board which contains a socket for the array, clock driver circuits, and a pre-amplifier.

Different array boards are needed for the various types of arrays:

RL-128C	--	RC-101	RL-128EC	--	RC-101
RL-256C	--	RC-101	RL-256EC	--	RC-102
RL-512C	--	RC-102	RL-512EC	--	RC-103
RL-768C	--	RC-103	RL-384EC	--	RC-103
RL-1024G	--	RC-103			
RL-128G	--	RC-104	RL-1024H	--	RC-107
RL-256G	--	RC-104	RL-1728H	--	RC-108
RL-512G	--	RC-105	RA-50x50A	--	RC110-01
RL-1024G	--	RC-106	RA-32x32A	--	RC110-02

The array boards are connected to the RC-100B Motherboard via connector J1/P1, or an optional 16-pin, 30 inch maximum, flat ribbon cable can be used. J1 is the 16-pin connector located approximately in the center of the RC-100B board. P1 is the male mating connector located on the array board. P2 is the edge connector of the RC-100B board.

INTERNAL/EXTERNAL CLOCK OPERATION

The RC-100B Motherboard contains an internal clock generator which supplies the master timing signal. Provisions are also made for an external clock input.

For internal clock operation, jumper INT CLOCK. The frequency range of the internal clock is controlled by the selection of capacitors C1-A and C1-B. Refer to Table A of Drawing Number 011-0238 for values for desired frequency range. R2, a 50K pot will allow for variance of the frequency within the selected frequency range. Boards are shipped from the factory with the clock frequency set at approximately 500KHz internal operation

For external clock operation, jumper EXT CLOCK, and apply an external clock into P2-Z. The external clock pulse should be an active TTL high clock with a minimum pulse width of 20ns, and a maximum pulse width of 200 μs.

INTERNAL/EXTERNAL START OPERATION

The RC-100B Motherboard contains an internal start pulse generator. Provisions for an external start pulse are also available.

For internal start operation, jumper INT START and set the desired interval between the start pulses, using the three four-position rocker switches S1, S2, and S3. Each switch has a weight of 2^n and a maximum count of 4096 is available. For optimum operation, the scan time should not exceed 40ms, because dark current increases with longer integration time. The minimum count between start pulses is eight, plus the number of elements in the array. Boards are shipped from the factory set in this configuration.

NOTE

If a scan time of >5 ms is used, change C28 on the RC-100B board to a .1μf capacitor.

Because of an inherent count of one in the start pulse generator, the setting on the rocker switches will be one less than the actual count, i.e., if a count of 520 is desired, set the rocker switches to 519.

The blanking period (time between last element of previous scan and first element of next scan) is defined as the count of the start pulse generator minus the number of elements in the array.

For external start operation, jumper EXT START and inject an external start signal into P2-A. The external start should be an active high TTL pulse with a minimum pulse width of the clock pulse width plus 50ns, and a maximum pulse width of less than one clock period.

If an external start is used, it should be synchronized with the negative-going edge of the clock to insure that the start pulse envelopes one and only one positive transition of the clock pulse.

POWER REQUIREMENTS

Connect +5 volts @ 700ma and -15 volts @ 300ma to P2-E and P2-Y, respectively. Connect ground to any pin from P2-1 to P2-22.

SECTION I

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC-101, 102, OR 103 AND FOUR PHASE "C" ARRAY

1. Jumper Connections. Split pads are provided to program the RC-100B board for the desired configuration. Refer to Table B of Drawing Number 011-0238 for correct configuration. See Figure 1 for location of split pads. Place the 2ø/4ø jumper in the 4ø position.

2. Monitor TP1 and adjust R2 (if internal clock is used) for the desired frequency. The maximum frequency is 2MHz. Adjust R11 for a 300ns, negative going pulse width.

3. Monitor P2-B and set the desired start pulse interval (if internal start is used). Synchronize the scope at P2-B during alignment.

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Monitor J1, Pin 1 (connector between array board and Motherboard). Darken the array and adjust R4 (pot on component side of the array board) until the video signal is centered around -5V dc. Saturate the array, readjust, if necessary, so no signal or switch spike is more negative than -8V dc. Do not over saturate.

6. Monitor J2-N (video output). The video output will be a sample-and-hold boxcar type signal.

7. Darken the array and adjust R36 until the average video is centered around the blanking period. (During blanking time, the video line is clamped to zero).

8. R50, R51, and R52 control the odd/even pattern balance. With the array in complete darkness, adjust R51 for equal amplitude of the odd video elements.

9. With the array still in the dark, adjust R52 for equal amplitude of the even video elements.

10. With the array still in the dark, adjust R50 for equal amplitude of the odd and even elements. There is some interaction between R51, R52 and R50. Repeat Steps 8, 9, and 10 until the desired degree of balance is obtained.

11. With the array still in darkness, adjust R32 until the first two video elements are as close in amplitude as possible to the other elements.

12. Monitor P2-N. Adjust R11 until optimum performance is observed at the video output. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation. If clock frequency is below 500KHz, R11 should be fully clockwise. This adjustment will interact with all the previous adjustments. Go back to Step 7 and touch up as necessary.

SECTION II

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC-101, 102, OR 103 WITH "EC" ARRAY

1. Jumper Connections. Refer to Table B of Drawing Number 011-0238 for correct configuration. See Figure 1 for location of split pads. Place the 2Ø/4Ø jumper in the 2Ø position.

2. Monitor TP1. Adjust R2 for desired frequency (if internal clock is used). Maximum frequency is 2 MHz. Adjust R11 for a 300ns, negative going pulse width.

3. Monitor P2-B. Set desired start pulse interval using rocker switches S1, S2, and S3 (if internal start is used).

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Monitor J1, pin 1. With the array in complete darkness, adjust R4 (pot on component side of array board) until the video is centered around -5V dc. Saturate the array, readjust, if necessary, so no signal or switching spike is more negative than -8V dc. Do not over saturate.

6. Monitor P2-N. Video output signal will be a sample-and-hold boxcar signal.

7. Darken the array and adjust R36 until the video elements are centered around the blanking level. (The blanking period is clamped to zero.)

8. With the array still in the dark, adjust either R51 or R52 until every other element is the same amplitude. (One of these pots will have no effect on the video signal.)

9. With the array still in the dark, adjust R50 to bring the odd and even elements together.

10. With the array still in the dark, adjust R32 (pot on the Motherboard) until the first two elements are as close to the same amplitude as the other elements as possible.

11. Adjust R11 until optimum performance is observed. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation. If clock frequency is below 500KHz, R11 should be fully clockwise.

12. Due to interaction between all the previous adjustments, return to Step 7 and realign until the desired response is achieved.

SECTION III

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC-104, 105, OR 106 AND "G" SERIES ARRAY

1. Jumper Connections. Split pads are provided to program the Rc-100B board for the desired configuration. Refer to Table B of Drawing Number 011-0238 for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1. Adjust R2 for the desired frequency, 1MHz maximum. Adjust R11 for a 700ns, negative going pulse width.

3. Monitor P2-B. Set the desired start pulse interval, using rocker switches S1, S2, and S3.

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Darken the array, monitor J1-I and adjust R4 (pot on the component side of the array board) to where the video signal is approximately centered at -5V dc. Saturate the array, readjust R4, if necessary, so no signal or or switching spike is more negative than -8V dc. Do not over saturate.

NOTE

Potentiometer R51, R52, R50 and R32 have no effect when the RC-100B is used in conjunction with a "G" series array board.

6. Monitor P2-N. The video output will be a sample-and-hold boxcar signal.

7. Darken the array and adjust R36 until the video signal is centered around the blanking level. (Blanking is clamped at zero.)

8. Adjust R11 until optimum performance is observed on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation.

9. With the array in dark, readjust R36 if necessary to bring the video level with the blanking.

SECTION IV

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC-107 OR 108 AND "H" SERIES ARRAY

1. Jumper Connections. Split pads are provided to program the RC-100B board for the desired configuration. Refer to Table B of Drawing Number 011-0238 for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1 and adjust R2 (if internal clock is used) for the desired frequency. The maximum frequency is 1.5MHz. Adjust R11 for a 200ns, negative going pulse width.

3. Monitor P2-B and set the desired start pulse interval (if internal start is used). Synchronize the oscilloscope at P2-B during alignment.

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Monitor J1-I. With the array in dark, adjust R24, (1K pot on the array board) to zero the base line of the video. Saturate the array and readjust R24, if necessary, so no signal or switching spikes go more negative than -8V dc. Do not over saturate.

NOTE

R51, R52, R50, and R32 on the RC-100B board will have no effect when an "H" series array board is used.

6. With the array still in dark, adjust R7 (200 Ω pot on the array board) for best odd/even pattern.

7. Monitor the video output at P2-N. With the array in dark, adjust R36 on the Motherboard until the video is centered with the blanking level.

8. Adjust R25 (100K pot on the array board) until the first three video elements are as close in amplitude as possible to the other elements.

9. Adjust R11 until optimum performance is derived on the video. Optimum adjustment of R11 resulting in a balance of maximum video output, minimum switching spikes, and a fixed pattern tracking from dark to 90% of saturation. This adjustment will interact with the previous adjustments. Go back to Step 5 and touch up as necessary.

SECTION V

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC100A-2 WITH RA32x32A ARRAY OR RC110A-1 WITH RA50x50 ARRAY

1. Jumper Connections. Split pads are provided to program the RC-100B board for the desired configuration. Refer to Table B of Drawing Number 011-0238 for proper configuration.

2. Monitor TP1. Adjust R2 for desired frequency. Maximum frequency is 1 MHz. Adjust R11 for a 600ns negative going pulse width.

3. Monitor P2-B. Set desired start pulse interval using rocker switches S1, S2, and S3 (if internal start is used). Start pulse interval must be at least 41 clock periods for a RA32x32A or 59 cloci periods for a RA50x50, giving a minimum line "flyback" of 9 clock periods.

4. Monitor TP2 and adjust R64 for a 100ns pulse width, sync scope at EOF terminal on the array board.

5. Monitor J1-I. With the array incomplete darkness, adjust R13 (potentiometer on component side of array board) until the video is centered around -5V dc. Saturate the array, readjust, if necessary, so no signal or switch spike is more negative than -8V dc. Do not over saturate.

6. Monitor P2-N, darken the array adn adjust R36 until the video elements are centered around the blanking level. (The blanking period is clamped to zero).

7. Adjust R11 until optimum performance is derived on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation.

8. The first element of each line is always low in amplitude. The second element's amplitude can be corrected by shorting out CR1, CR2 and/or CR3. This will vary with arrays and may require none, one, two or all of these shorted out for best results.

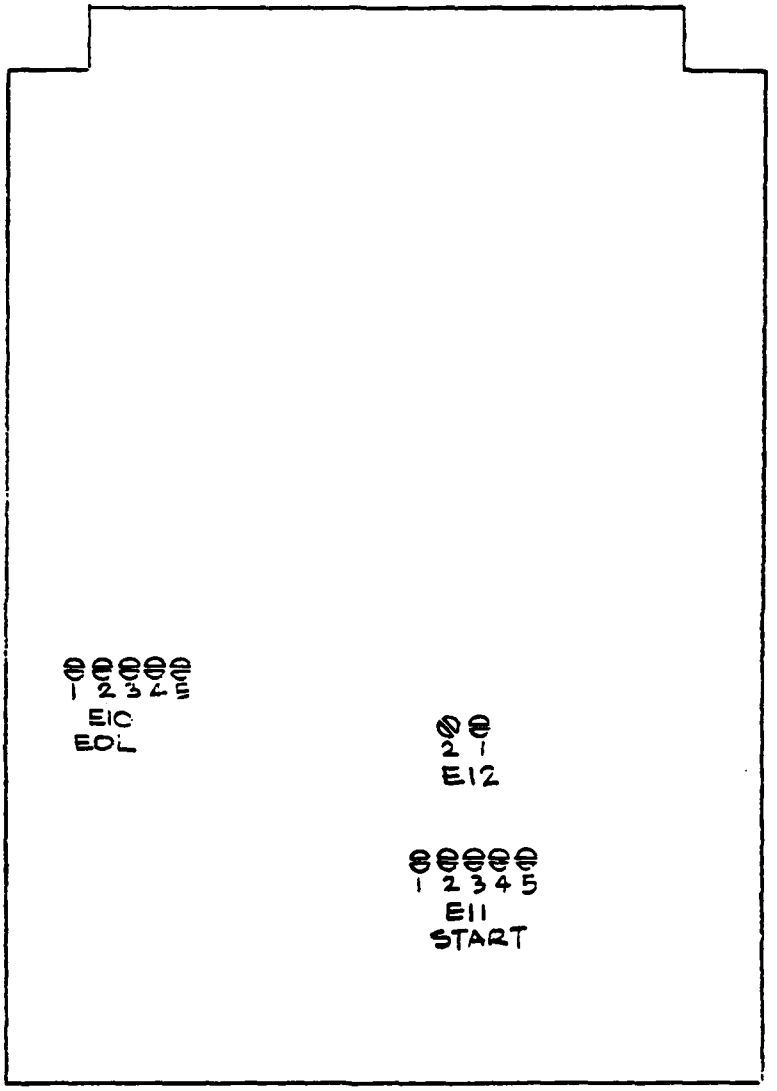
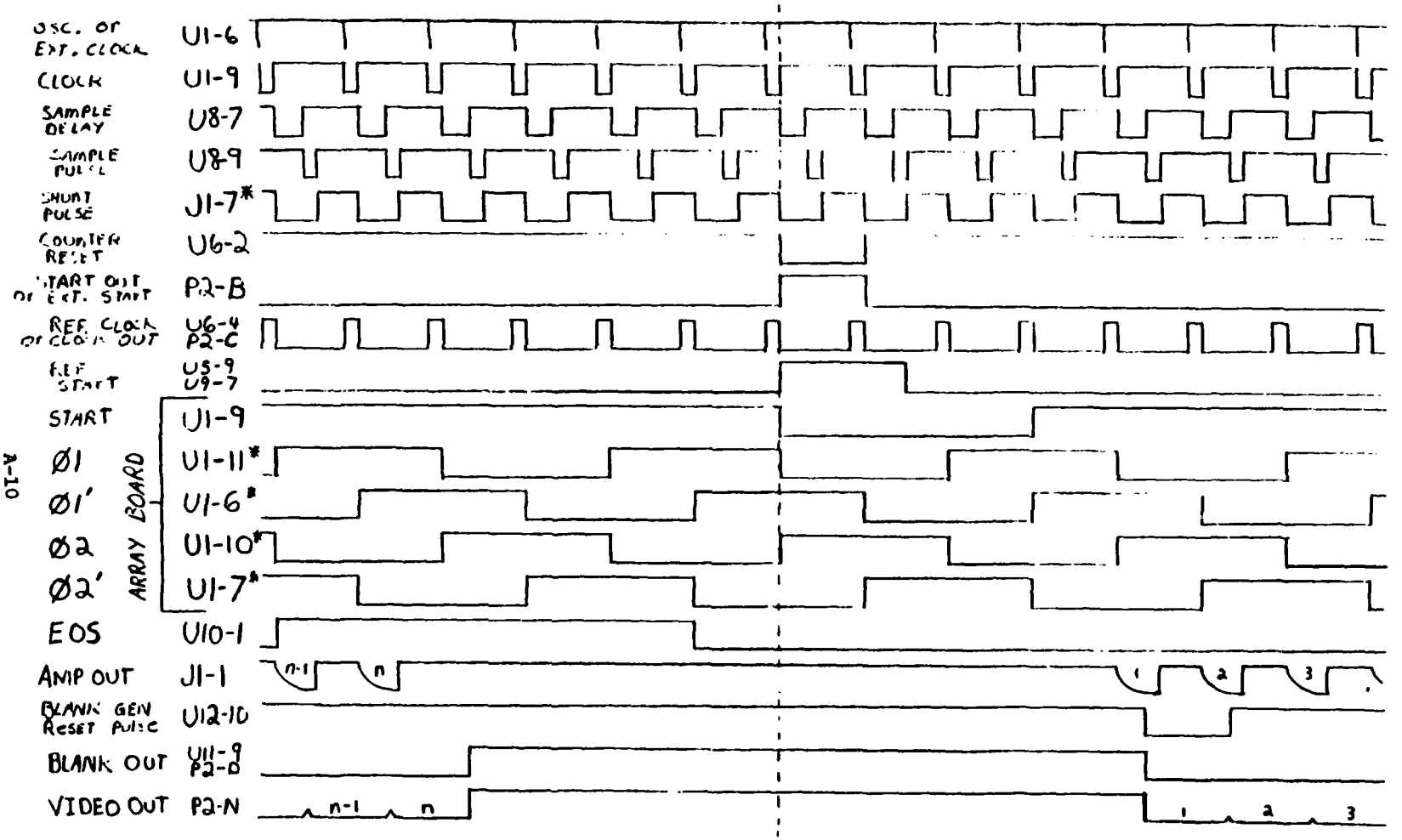


Figure 1 Split Pad Location

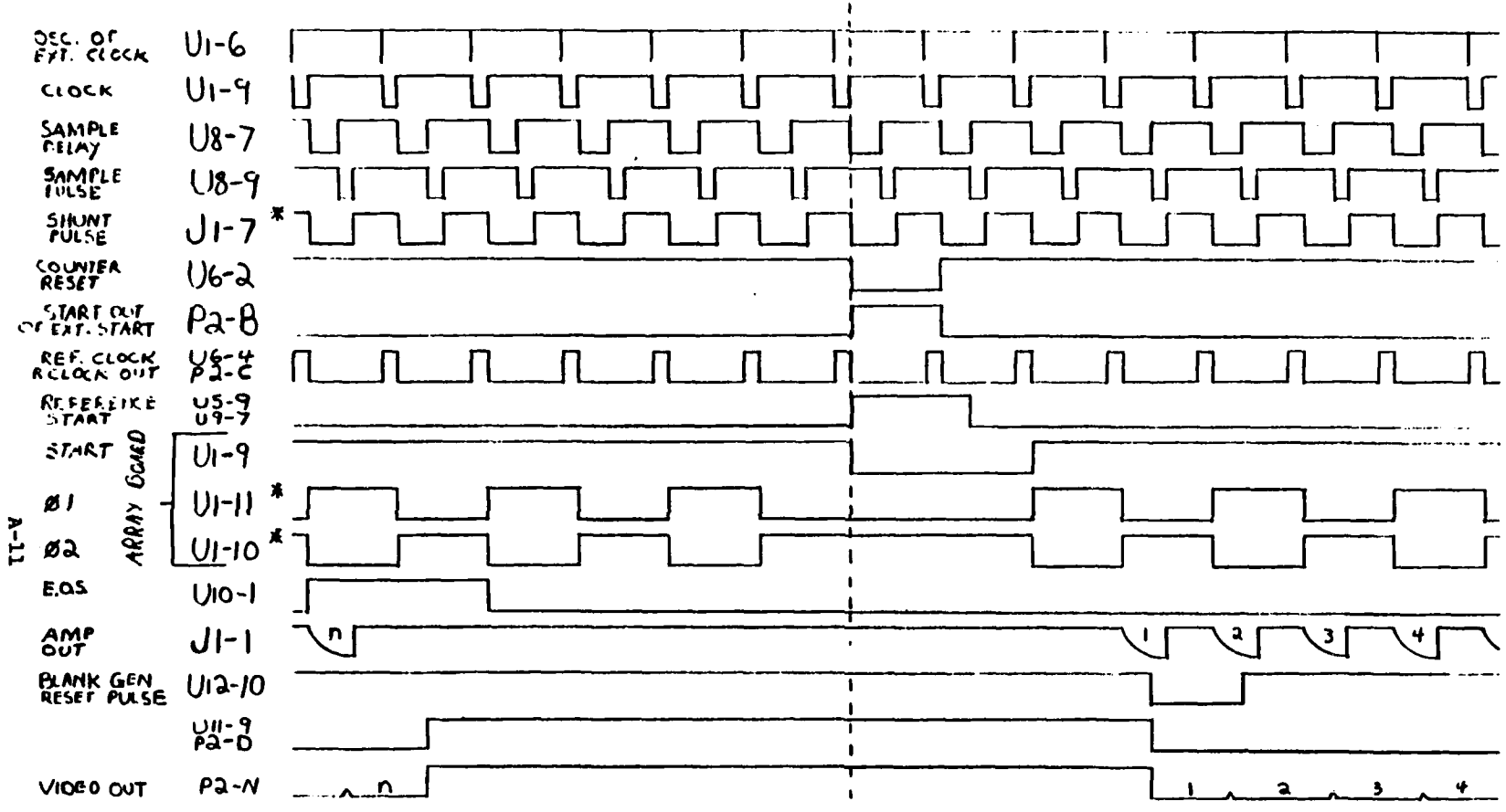
RETICON	RETICON CORPORATION 910 Benecia Ave. Sunnyvale California 94086	SIZE A	DRAWING NO. 045-0050	SHEET 9 OF 9

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-5271



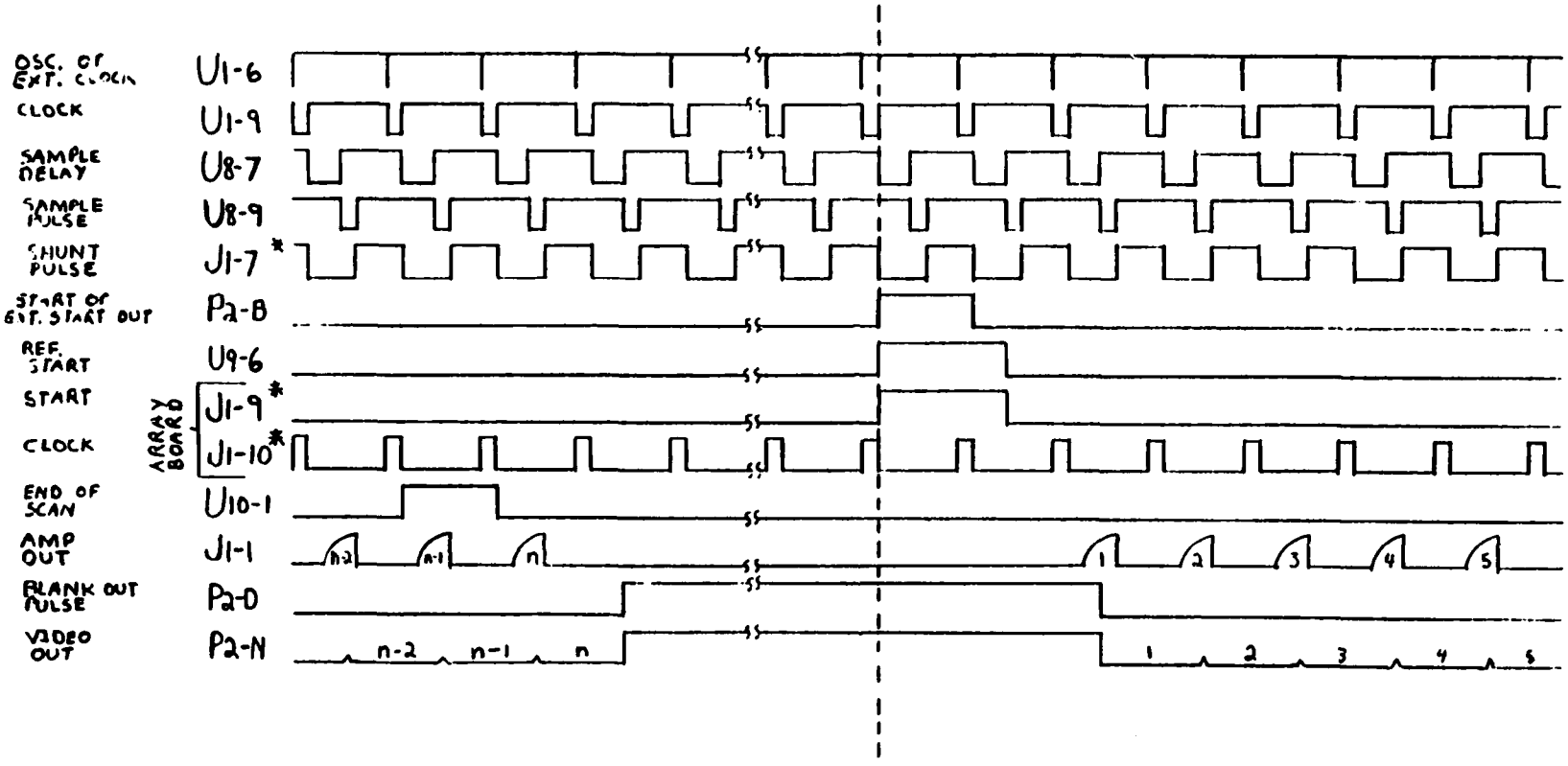
* Denotes MOS Level Signals, ALL Other Except Video Are TTL

Timing Diagram
RC-108B Series Circuit Boards
4 Phase Operation
C Series Array



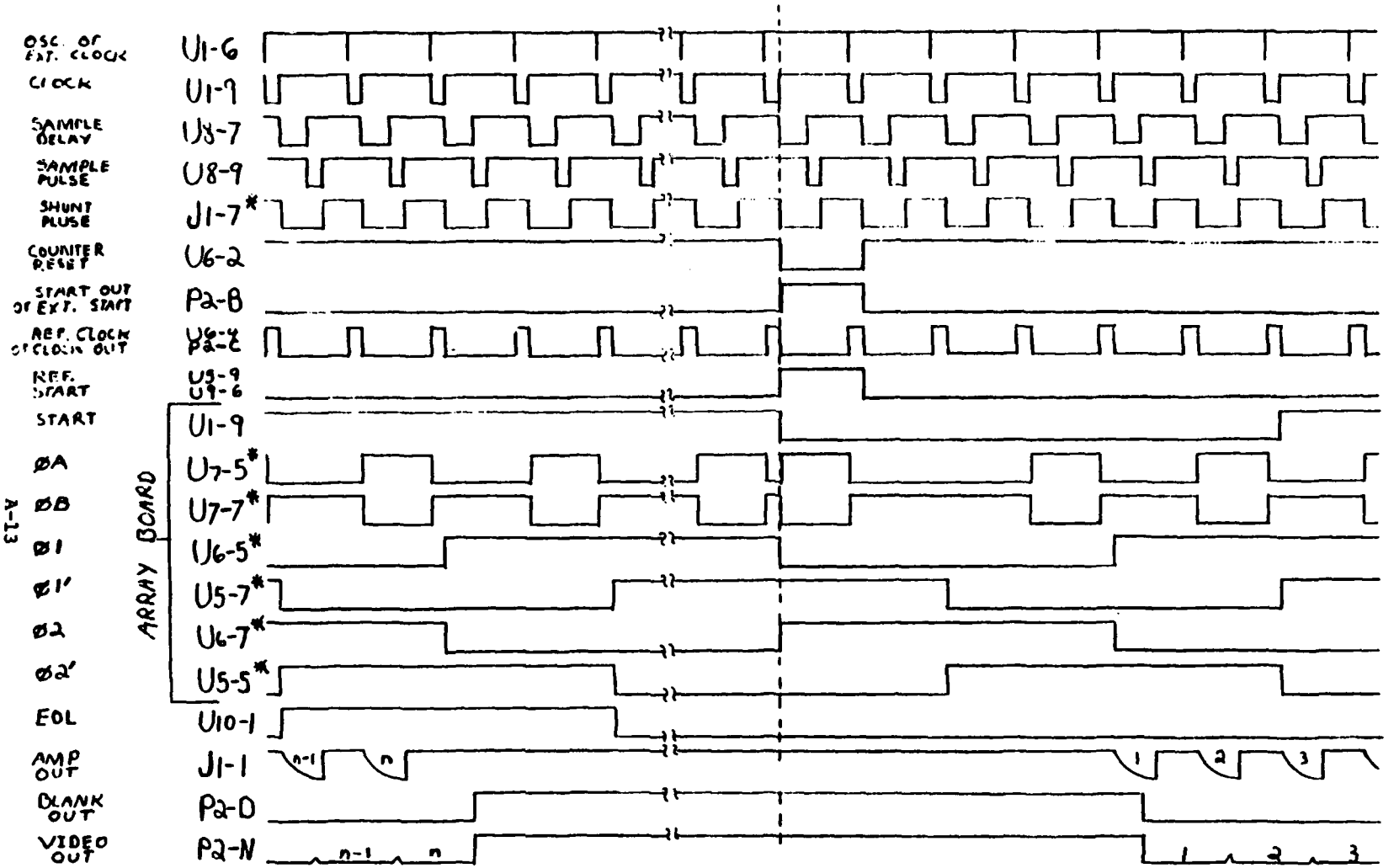
*Denotes MOS Level Signals, ALL Other Except Video Are TTL

Timing Diagram
RC-100B Series Circuit Boards
2 Phase Operation
EC Series Array



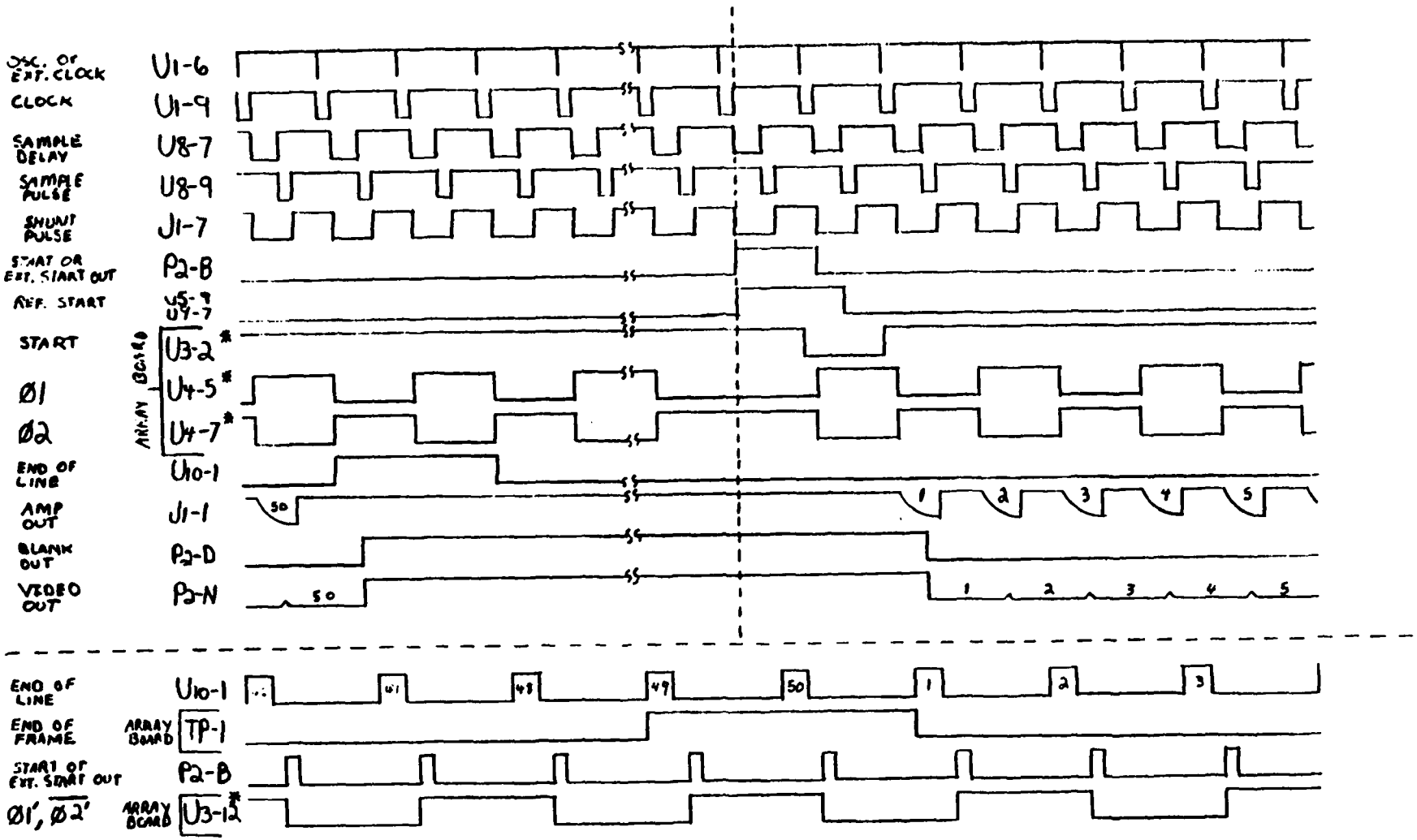
* Denotes MOS Level Signals, ALL Other Except Video Are TTL

Timing Diagram
RC-100B Series Circuit Boards
G Series Array



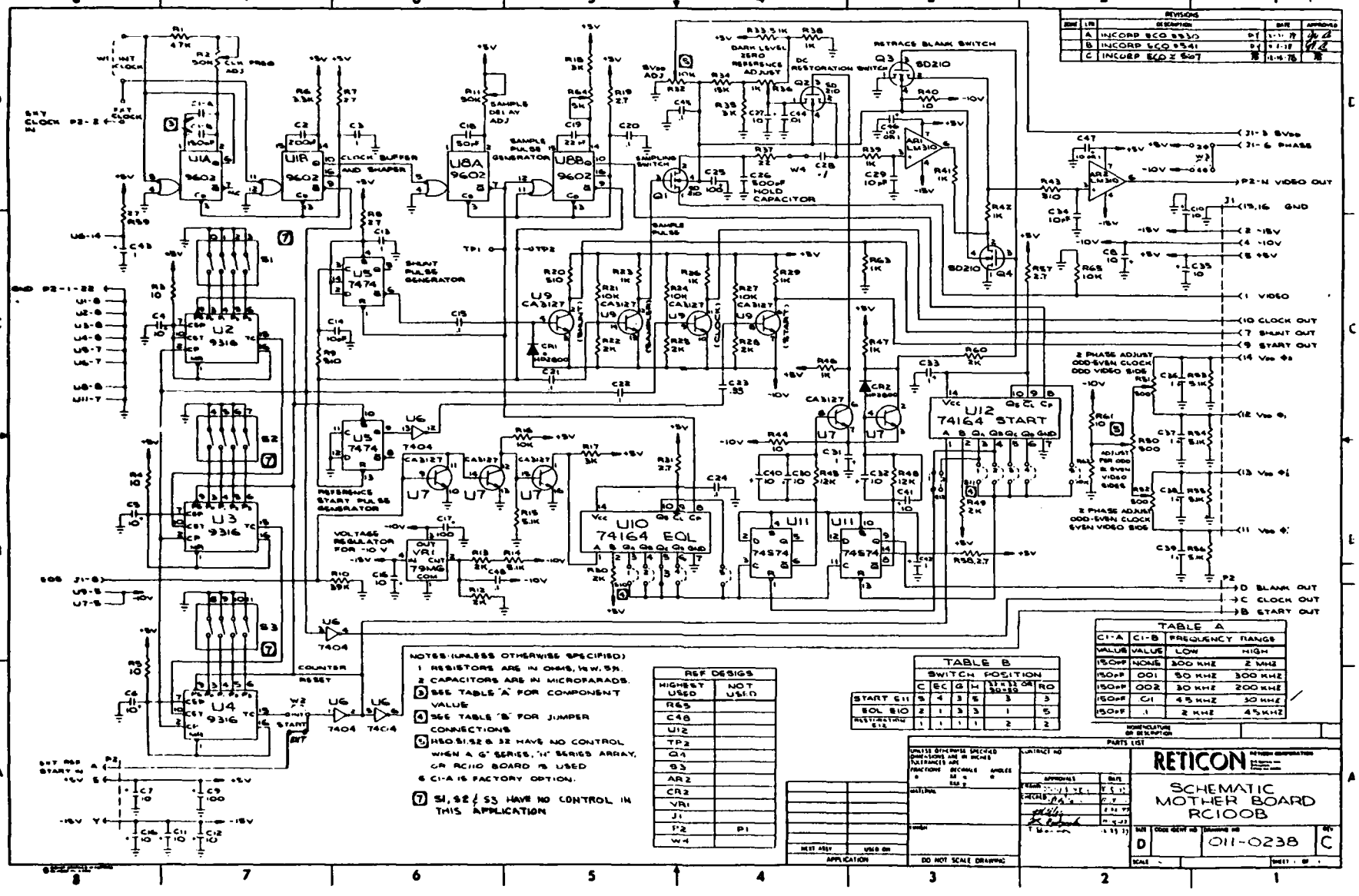
* Denotes MOS Level Signals. ALL Other Except Video Are TTL

Timing Diagram
RC-100B Series Circuit Boards
H Series Array



* Denotes Mos Level Signals. All Other Except Video Are TTL

Timing Diagram
RC-180B Series Circuit Boards
RA-50x50 Array



NOTES: (UNLESS OTHERWISE SPECIFIED)
1 RESISTORS ARE IN OHMS, ¼W, 5%.
2 CAPACITORS ARE IN MICROFARADS.
3 SEE TABLE "A" FOR COMPONENT VALUE
4 SEE TABLE "B" FOR JUMPER CONNECTIONS
5 R50, S1, S2 & S3 HAVE NO CONTROL WHEN A "G" SERIES, "H" SERIES ARRAY, OR RC110 BOARD IS USED
6 C1-A IS FACTORY OPTION.
7 S1, S2 & S3 HAVE NO CONTROL IN THIS APPLICATION

REF DESIGS	
HIGHEST USED	NOT USED
R65	
C48	
U12	
TP2	
Q4	
S3	
AR2	
CR2	
VR1	
J1	
P2	P1
W4	

TABLE B

	SWITCH POSITION					
	C	EC	G	H	S1 & S2 OR S0-S3	RO
START E11	5	4	3	5	3	3
EOL E10	2	1	3	3	1	5
RESTORATION E12	1	1	1	1	2	2

TABLE A

C1-A	C1-B	FREQUENCY RANGE	
VALUE	VALUE	LOW	HIGH
150pF	NONE	300 KHZ	2 MHZ
150pF	.001	50 KHZ	300 KHZ
150pF	.002	30 KHZ	200 KHZ
150pF	.01	4.5 KHZ	30 KHZ
150pF	.1	2 KHZ	4.5 KHZ

NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ± DECIMALS ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS | DATE

DRAWN

CHECKED

T. Bowen

RETICON RETICON CORPORATION

SCHEMATIC
MOTHER BOARD
RC100B

SIZE D | CODE IDENT NO | DRAWING NO 011-0238 | REV C

SCALE | SHEET 1 OF 1

APPENDIX B
Z-80 EDGE CARD SYSTEMS
PLS-898 ONE CARD SYSTEM

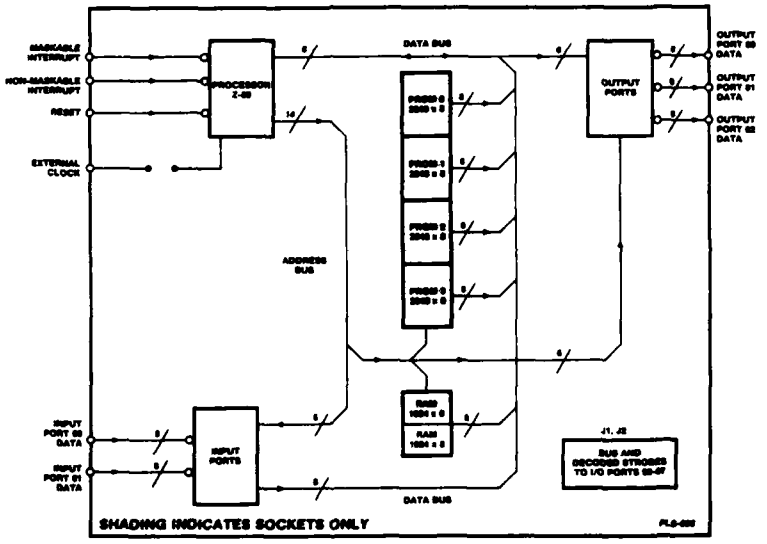
Z-80 EDGE CARD SYSTEMS
PLS-898 ONE CARD SYSTEM

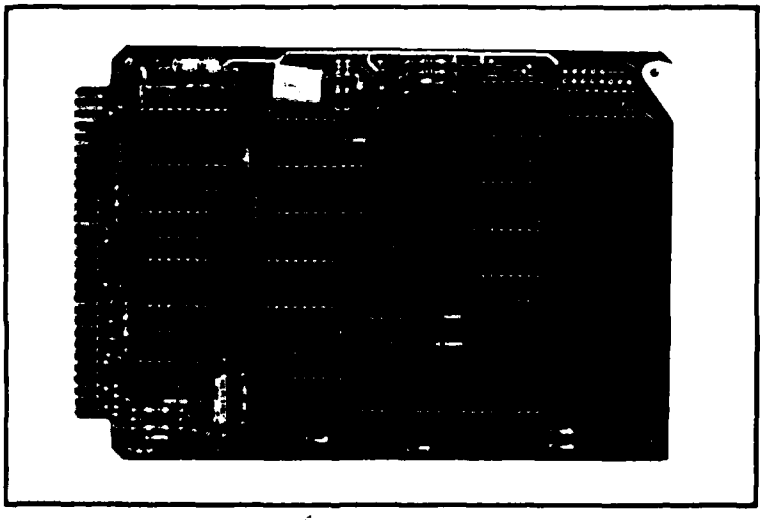
The PLS-898 is a complete Z-80 microprocessor system on one 4½" x 6½" circuit card. The system provides a 56-pin card edge connector that is pin compatible with the existing Pro-Log PLS-881 and PLS-886 microprocessors. The PLS-898 incorporates all the elements of the highly popular PLS-881 and expands on them. The PLS-898 offers the capability of expanding program memory to 8192 bytes using 2048 byte D2002 PROM (2716 or equivalent). The PLS-898 also comes with 1024 bytes of read/write memory but can be expanded to 2048 bytes simply by plugging in two additional D1004 RAM's (2114 or equivalent). Like the companion PLS-881, the more powerful PLS-898 includes three output ports and two input ports at the card edge; however, I/O can be expanded to eight input and eight output ports with a simple ribbon cable expansion system that accesses the data bus and I/O decoder strobes. The PLS-898 operates from a single +5V supply.

The PLS-898's Z-80 Processor includes all of the 8080A instructions as a subset, and adds Bit, Relative, and Indexed addressing modes, powerful data block search and move instructions and a duplicate set of internal registers. The PLS-898 can significantly reduce program memory storage requirements and execution time in many applications.

FEATURES

- **Z-80 Processor**
- **2K Byte RAM Capacity with 1K Included**
- **Sockets for 8K Bytes 2716 EPROM**
- **Crystal Clock**
- **400 Nanosecond State Time**
- **Three 8-Bit Output Ports**
- **Two 8-Bit Input Ports**
- **External Port Expansion to 16 Ports**
- **Two Interrupts**
- **Single +5V supply**





PLS-898 ONE CARD SYSTEM

PROGRAM MEMORY: PROM

PLS-898 program memory consists of one to four 2716 erasable PROM devices. Each 2716 contains 2048 eight-bit words organized as eight 256-word memory pages. PLS-898 program memory is assigned consecutive page locations as follows:

PROM NUMBER	OCCUPIES HEX MEMORY PAGES
0	00 to 07
1	08 to 0F
2	10 to 17
3	18 to 1F

DATA MEMORY: RAM

RAM data memory consists of two (standard) or four (optional) 2114 RAM devices. The 2114 is a 1024 x 4 RAM; each pair of 2114's provides 1024 eight-bit words organized as four 256-word memory pages. The standard PLS-898 provides RAM memory in pages 20 through 23. Two additional 2114 devices add RAM pages 24 through 27; these are implemented by plugging the devices in the sockets provided on the PLS-898 card.

RAM NUMBER	OCCUPIES HEX MEMORY PAGES
1, 2 (standard)	20 to 23
3, 4 (optional)	24 to 27

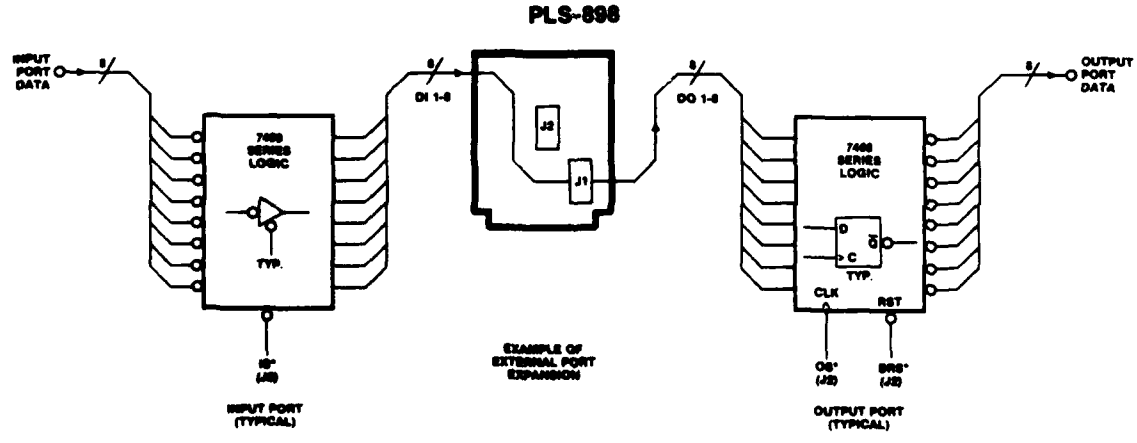
ON-CARD I/O PORTS

The PLS-898 provides two eight-bit input ports and three eight-bit output ports. These ports provide 16 input lines and 24 output lines available at the edge connector and are TTL compatible.

ON-CARD PORT ADDRESSES (HEX)	
INPUT PORTS	00 and 01
OUTPUT PORTS	00, 01, and 02

PORT EXPANSION: DIRECT

PLS-898 can directly address additional I/O via two 16 pin dip sockets (J1 and J2). Dip connector terminated cables can be used to interconnect either existing Pro-Log I/O circuit boards such as 8114 and 8115-1 or user designed I/O boards such as A/D and D/A converters, UART and USARTs. The PLS-898 can access an additional six 8-bit input and five 8-bit output ports or devices in this manner. The control signals provided at J2 are input and output select lines which combine a decoded port address with the Z-80's port Read or Write and timing signals. The Input Select lines (IS-2* through IS-7*) are applied directly to 3-state enable pins to gate data to the Data In Bus (J1, DI-1 through DI-8); the Output Select lines (OS-3* through OS-7*) normally clock output port latches loaded by the Data Out Bus (J1, DO-1 through DO-8). The following are examples of external I/O port implementation:



*Denotes Low Level Active Logic

I/O PORT EXPANSION: MULTIPLEXING

A large number of external I/O ports may be multiplexed through the on-card PLS-898 I/O ports. However, this type of expansion requires more Processor execution time because each I/O operation must be preceded by an output instruction which selects the port and followed by output instructions which provide the output strobes.

In this technique, one PLS-898 on-card Input port and one Output port are committed for use as data in and out busses. Other output port lines are used as I/O port select, port card select and port strobes as required.

INTERRUPT

The PLS-898 has two low activated, level sensitive interrupts with several designer options:

Nonmaskable Interrupt (NMI*) has the highest priority and cannot be disabled.

Interrupt Request (IREQ*) is enabled/disabled by the (EIN)/(DIN) instructions. The user can select one of three modes which define the action taken when IREQ* is honored:

Mode 0 - Execute any instruction at Interrupt, but the instruction must be supplied by the interrupting device to the data in bus (DI 1-8), J1.
Mode 1 - Execute the RST 38 instruction.
Mode 2 - Restart at any memory address acording to a selected address vector (16 bits) stored in two memory locations. The interrupting device must supply the even line number of the first 8 bits of the restart address vector; the page address is previously loaded by the program.

Modes 0 and 1 are summarized by the following table. The Pro-Log 8118-1 Priority Interrupt card supplies one of eight RST instructions according to the active interrupt request to support Mode 0:

	INTERRUPT	PRIORITY	RESTART ADDRESS (HEX)	MODE
PLS-898	NONMASKABLE	HIGHEST	PAGE 00 LINE 66	ANY
PLS-898	IREQ OR IREQ 7	SECOND HIGHEST	PAGE 00 LINE 38	1 / 0
8118-1 EXPANSION	IREQ 6	THIRD	PAGE 00 LINE 30	0
8118-1 EXPANSION	IREQ 5	FOURTH	PAGE 00 LINE 28	0
8118-1 EXPANSION	IREQ 4	FIFTH	PAGE 00 LINE 20	0
8118-1 EXPANSION	IREQ 3	SIXTH	PAGE 00 LINE 18	0
8118-1 EXPANSION	IREQ 2	SEVENTH	PAGE 00 LINE 10	0
8118-1 EXPANSION	IREQ 1	EIGHTH	PAGE 00 LINE 08	0
8118-1 EXPANSION	IREQ 0	LOWEST	PAGE 00 LINE 00	0

PLS-898 INTERRUPT EXPANSION SUMMARY

Z-80/8080A COMPATABILITY

The PLS-898 instruction set offers the PLS-881/888 (8080A-based) instructions as a subset. 8080A programs will execute normally in the PLS-898; however, the PLS-898 has shorter time states (400 ns) than the PLS-881/888 (488 ns), and certain Z-80 instructions execute in a different number of time states than identical 8080A instructions. Consequently, programmed timing adjustments may be necessary. Also, three Flag Register bits which were unused and constant in the 8080A are now used by the Z-80, and the Parity Flag assumes the dual role of Parity and Signed Binary Overflow with altered action after add and subtract instructions. Z-80 Interrupt Mode 0 is identical to the 8080A interrupt system.

The PLS-898 will execute PLS-858 (8085-based) programs except for the 8085's Read Interrupt Mask (RIM) and Set Interrupt Mask (SIM) instructions, with programmed timing adjustments as required.

The Z-80 Processor executes 158 instructions compared to the 8080A's 72. The additional Z-80 instructions are identified by first word HEX codes of 10, 18, 20, 28, 30, 38, CB, DD, ED, or FD, followed by 1, 2, or 3 more words. The following PLS-898 pin assignments are identical to the PLS-881 to minimize rewiring for system upgrade to the Z-80 Processor:

Input Port Lines
Output Port Lines
+5V and Ground
Reset Input and Output
RDY Input
Interrupt Request (IREQ*)

PLS-898 DESIGNER OPTIONS

The PLS-898 has 5 spare edge connector pins (5, 6, 52, 55, 56) which may be connected from pads provided to the following signals:

RESET (Active High Output)
EXTERNAL CLOCK INPUT (Remove PLS-896 Crystal)
DECODED PAGES 28-2F, 30-37, 38-3F (3 lines)
ADDRESS LINES A14, A15, A16
BUFFERED WRITE, BWR* (Active Low Output)

*Denotes Low Level Active Logic

CARD DIMENSIONS

- 4.50 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
- 0.48 in. (1.22 cm) maximum profile thickness
- 0.062 in. (0.16 cm) printed circuit board thickness

CARD INCLUDES

- Card ejector
- One Z-80 Processor
- 1K 8-bit bytes, 2114 RAM plus sockets for an added 1K bytes
- Four ROM sockets for 2716 PROMs
- Crystal clock circuit and provisions for external clock
- Power-on and external reset
- 2 Input ports (8-bit)
- 3 Output ports (8-bit)

INSTRUCTION EXECUTION CAPABILITY

- Executes all of the Z-80 Processor instructions
- 0.40 microseconds time state cycle ±0.05% at 25°C; ±0.1% 0-55°C
- Instructions require from 4 to 23 times states

MEMORY

- Maximum Access Time: 0.450 microseconds
- PROM: 2716 or equivalent
- RAM: 2114 or equivalent

INPUTS (Active low logic, loading 1 LSTTL load, except where noted.)

- 2 Interrupt requests
- 16 Data lines (2 input ports)
- 1 RDY control (active high)
- 1 Reset Control
- Port Expansion Data Bus (J1; active high)
- External clock input

***OUTPUTS** (Active low logic, drive capability 5 TTL loads, except where noted.)*

- 24 Latched Output Data lines (3 output ports)
- 1 clock signal
- 2 system resets (J2 and card edge)
- Port Expansion Data Bus (J1; active high)
- 6 Input ports strobes (J2)
- 5 Output port strobes (J2)

POWER REQUIREMENTS

+VCC = +5 volts ±5% at 1.2 A maximum fully loaded (100 mA per ROM, 100 mA per RAM)
GND = 0 volts

***OPERATION TEMPERATURE RANGE:** 0-55°C*

CONNECTOR REQUIREMENTS:

56 pin, 28 position dual-readout on 0.125 in. (0.318 cm) centers

PLS-898 EDGE CONNECTOR PIN LIST

PIN NUMBER SIGNAL FLOW SIGNAL			PIN NUMBER SIGNAL FLOW SIGNAL		
+5 VOLTS	IN	2	1	IN	+5 VOLTS
GROUND	IN	4	3	IN	GROUND
SPARE	I/O	6	5	I/O	SPARE
IN0-6*	IN	8	7	IN	IN1-5*
IN0-6*	IN	10	9	IN	IN1-6*
IN0-7*	IN	12	11	IN	IN1-7*
IN0-8*	IN	14	13	IN	IN1-8*
IN0-4*	IN	16	15	IN	IN1-4*
IN0-3*	IN	18	17	IN	IN1-3*
IN0-2*	IN	20	19	IN	IN1-2*
IN0-1*	IN	22	21	IN	IN1-1*
OUT0-1*	OUT	24	23	OUT	OUT0-5*
OUT0-2*	OUT	26	25	OUT	OUT0-6*
OUT0-3*	OUT	28	27	OUT	OUT0-7*
OUT0-4*	OUT	30	29	OUT	OUT0-8*
OUT1-1*	OUT	32	31	OUT	OUT1-5*
OUT1-2*	OUT	34	33	OUT	OUT1-6*
OUT1-3*	OUT	36	35	OUT	OUT1-7*
OUT1-4*	OUT	38	37	OUT	OUT1-8*
OUT2-1*	OUT	40	39	OUT	OUT2-5*
OUT2-2*	OUT	42	41	OUT	OUT2-6*
OUT2-3*	OUT	44	43	OUT	OUT2-7*
OUT2-4*	OUT	46	45	OUT	OUT2-8*
INTA*	I/O	48	47	IN	IREQ*
NMI*	IN	50	49	IN	RDY
SPARE	I/O	52	51	OUT	TTL0
RESET*	IN	54	53	OUT	RST*
SPARE	I/O	56	55	I/O	SPARE

*Designates Active Low Level Logic

I/O PORT EXPANSION SOCKETS

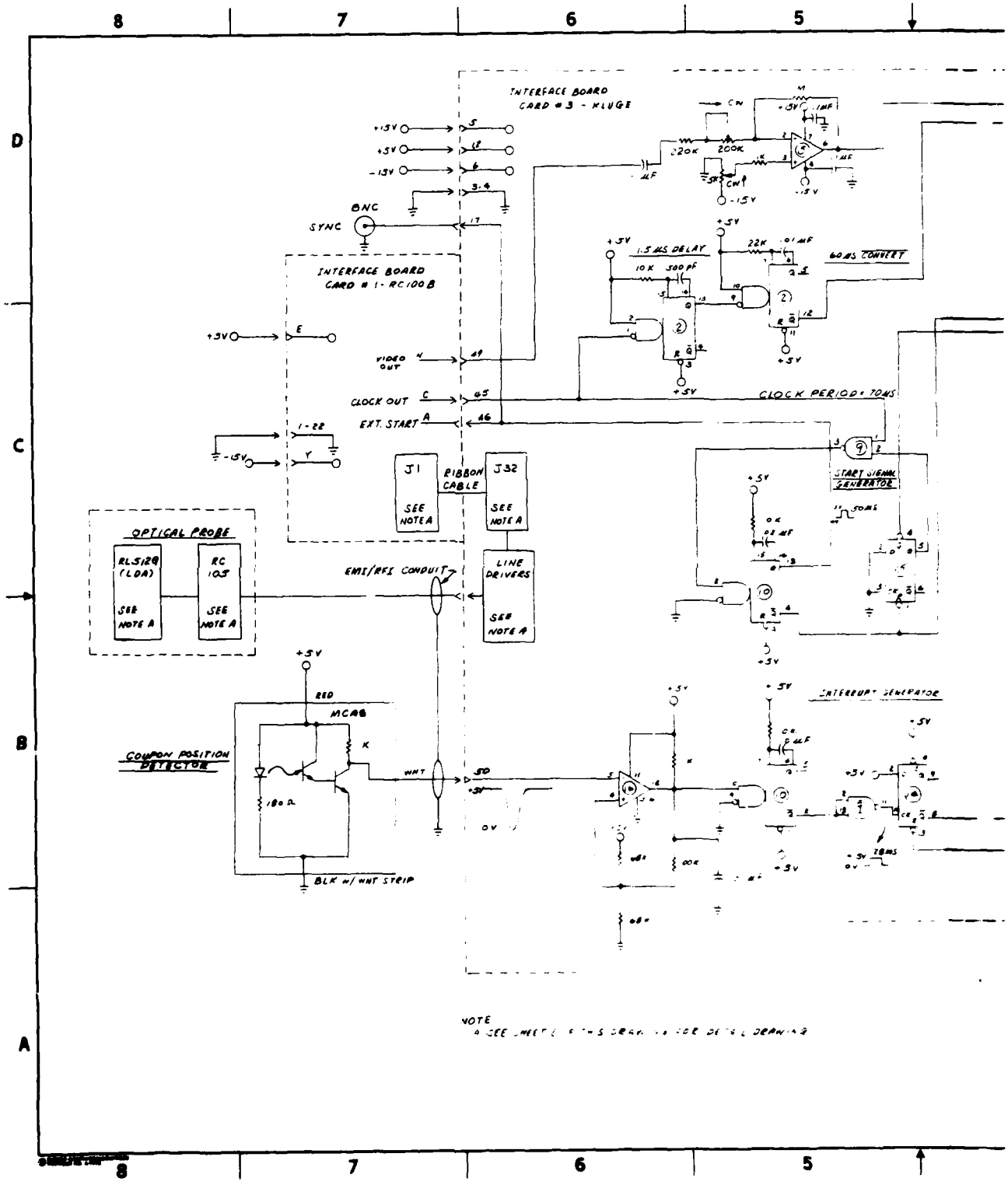
J1 DATA					
PIN NUMBER SIGNAL FLOW SIGNAL			PIN NUMBER SIGNAL FLOW SIGNAL		
DI-4	IN	16	1	IN	DI-1
DO-2	OUT	15	2	IN	DI-8
DO-4	OUT	14	3	OUT	DO-6
DO-1	OUT	13	4	OUT	DO-7
DI-7	IN	12	5	OUT	DO-3
DO-5	OUT	11	6	IN	DI-5
DO-8	OUT	10	7	IN	DI-6
DI-3	IN	9	8	IN	DI-2
J2 CONTROL AND POWER					
PIN NUMBER SIGNAL FLOW SIGNAL			PIN NUMBER SIGNAL FLOW SIGNAL		
GND	OUT	16	1	OUT	GND
IS-2*	OUT	15	2	OUT	BRS*
IS-3*	OUT	14	3	OUT	OS-3*
IS-4*	OUT	13	4	OUT	OS-4*
IS-5*	OUT	12	5	OUT	OS-5*
IS-6*	OUT	11	6	OUT	IS-7*
OS-6*	OUT	10	7	OUT	+5 VOLTS
OS-7*	OUT	9	8	OUT	+5 VOLTS

*Designates Active Low Level Logic

PRO-LOG
CORPORATION 2411 Garden Road Monterey, California 93940 Telephone (408) 372-4593
TWX: 910-360-7082

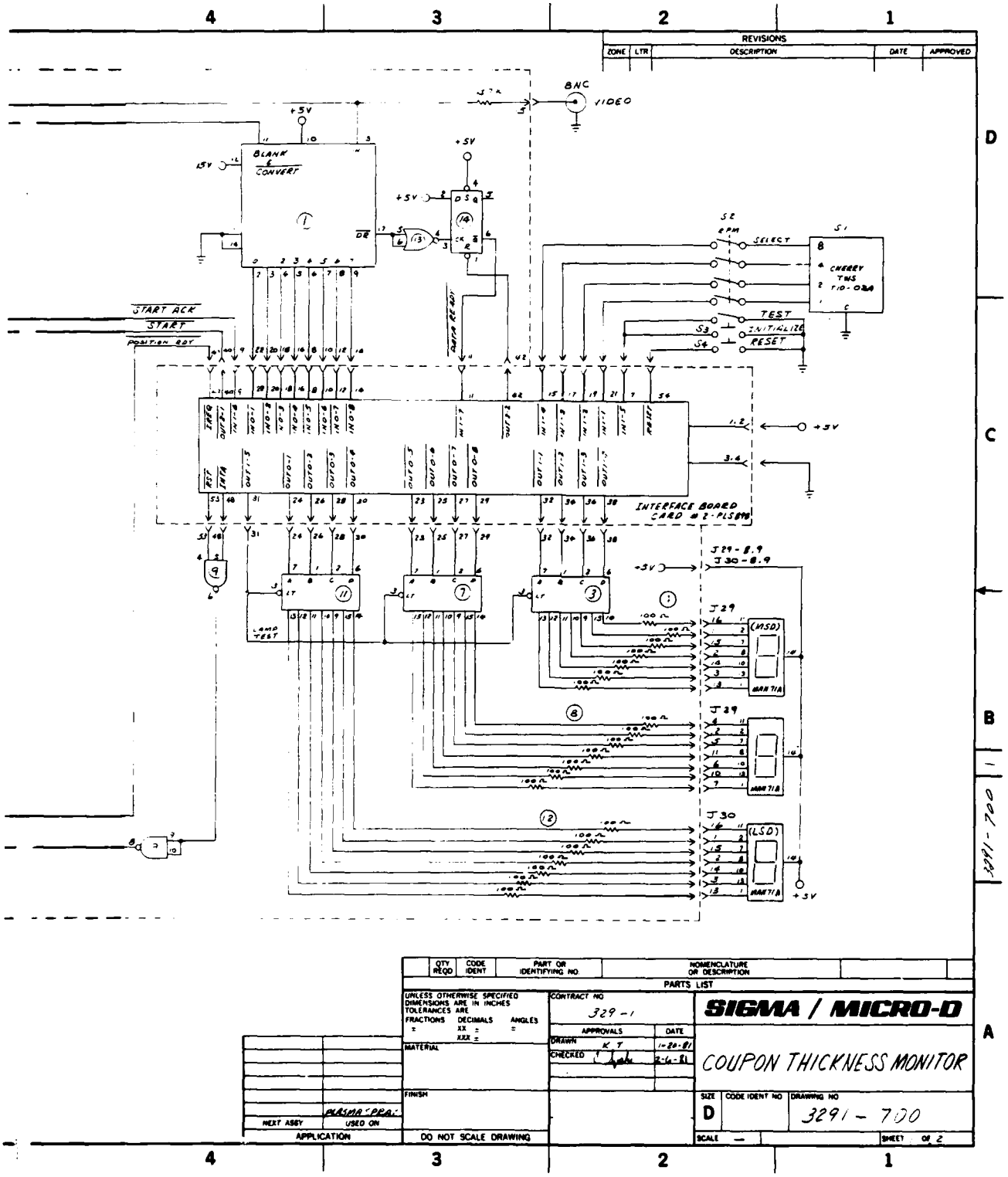
102695 3/78

APPENDIX C
SCHEMATICS



INTERFACE BOARD
CARD # 3 - KLUGE
+15V
+5V
-15V
BNC
SYNC
INTERFACE BOARD
CARD # 1 - RC100B
VIDEO OUT
CLOCK OUT
EXT. START
1.5 μS DELAY
60 μS CONVERT
CLOCK PERIOD = 70 μS
START SIGNAL GENERATOR
J1
SEE NOTE A
RIBBON CABLE
J32
SEE NOTE A
OPTICAL PROBE
RLS129 (LDA)
SEE NOTE A
RC 105
SEE NOTE A
EMI/RFI CONDUIT
LINE DRIVERS
SEE NOTE A
RED
MCAG
COUPON POSITION DETECTOR
WHT
BLK w/ WHT STRIP
INTERRUPT GENERATOR
NOTE

C1


REVISIONS
ZONE
LTR
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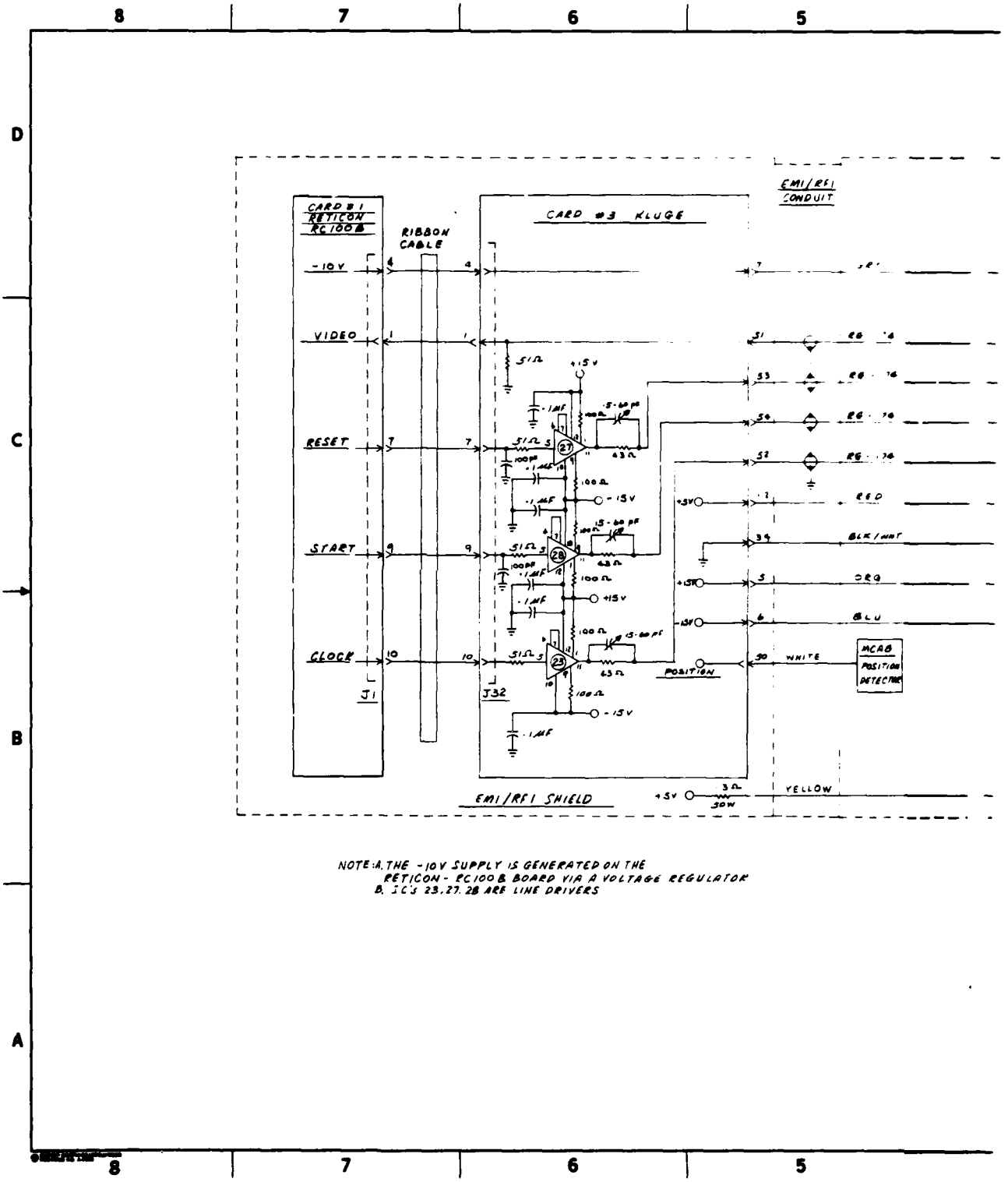
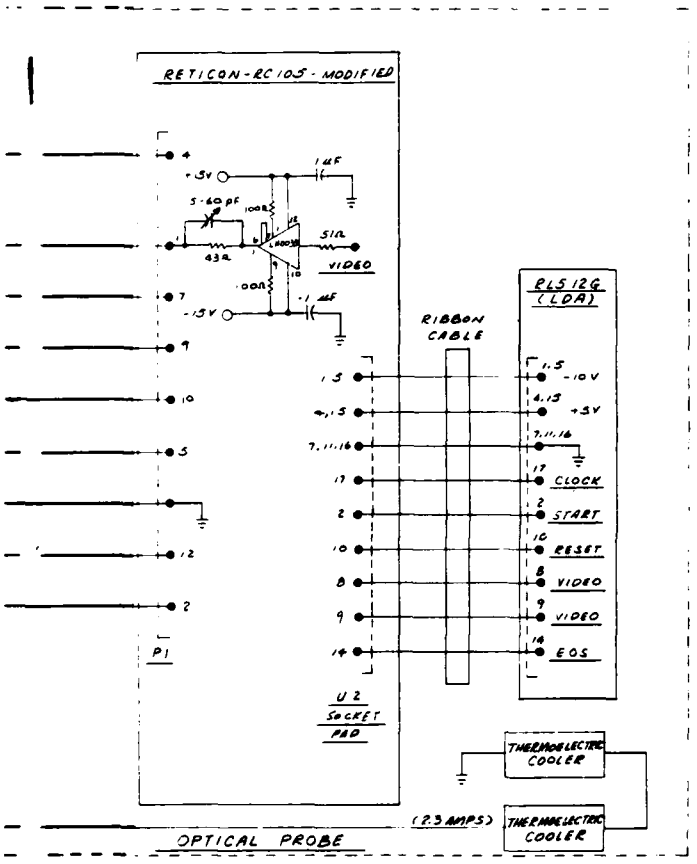
APPROVED
BNC
VIDEO
+5V
BLANK & CONVERT
15V
START ACK
START
POSITION RDY
DATA READY
S2
RPM
SELECT
S1
CHERRY TWS T10-02A
TEST
INITIALIZE
RESET
S3
S4
INTERFACE BOARD CARD # 2-PLS898
LAMP TEST
J29-8.9
J30-8.9
J29
(MSD)
MAN 71A
J30
(LSD)
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ±
DECIMALS XX ± XXX ±
ANGLES ±
MATERIAL
FINISH
CONTRACT NO
329-1
APPROVALS
DATE
DRAWN
CHECKED
1-20-81
2-6-81
SIGMA / MICRO-D
COUPON THICKNESS MONITOR
SIZE
D
CODE IDENT NO
DRAWING NO
3291 - 700
SCALE
SHEET OF 2
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
3291-700



NOTE: A. THE -10V SUPPLY IS GENERATED ON THE RETICON - RC100 B BOARD VIA A VOLTAGE REGULATOR
B. IC'S 23, 27, 28 ARE LINE DRIVERS



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

28	LH0033
27	LH0033
23	LH0033
16	LM319
15	7474
14	7474
13	7402
12	16-PIN HEADER
11	7447
10	74123
9	74LS132
8	16 PIN HEADER
7	7447
6	16-PIN HEADER
5	LM 318
4	16-PIN HEADER
3	7447
2	74123
1	AD 570
IC #	PART OR IDENTIFYING NO

3291-700

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON: PLASMA SPRAY

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO 329-1

APPROVALS	DATE
DRAWN K.T.	2-3-81
CHECKED	2-6-81

SIGMA / MICRO-D

LINE DRIVERS AND INTER-CONNECTIONS BETWEEN PLASMA SPRAY MONITOR AND OPTICAL PROBE

SIZE	CODE IDENT NO	DRAWING NO.
D		3291-700

SCALE — SHEET 2 OF 2

APPENDIX D
CALIBRATION OF THICKNESS MEASURING GAUGE

CALIBRATION OF THICKNESS MEASURING GAUGE

Start at Spot Position 400

Actual Position (mils)	Position Readout (mils)	Error (mils)	Actual Position (mils)	Position Readout (mils)	Error (mils)	Actual Position (mils)	Position Readout (mils)	Error (mils)
-50	-48	+2	80	80	0	210	208	-2
-40	-38	+2	90	88	-2	220	218	-2
-30	-28	+2	100	97	-3	230	228	-2
-20	-19	+1	110	110	0	240	238	-2
-10	-10	0	120	118	-2	250	248	-2
0	0	0	130	128	-2	260	258	-2
10	10	0	140	138	-2	270	268	-2
20	20	0	150	149	-1	280	280	0
30	28	-2	160	158	-2	290	291	+1
40	37	-3	170	169	-1	300	300	0
50	50	0	180	179	-1	310	311	+1
60	60	0	190	187	-3	320	321	+1
70	68	-2	200	198	-2			

$\overline{(\text{error}^2)} = 2.79\ (\text{mils}^2)$; $\left[\overline{(\text{error}^2)}\right]^{1/2} = 1.67\ (\text{mils})$

*Measurements were made on a Bridgeport mill equipped with a Sony Magnescale LF-200 digital readout with 0.0001 inch accuracy.

END

DATE
FILMED

9 - 83

DTIC